AiP74HC/HCT165
8-bit Parallel-in, Serial out Shift Register

Product Specification

Specification Revision History：

Version	Date	Description
2012-07-A1	2012-07	New
2023-04-B1	2023-04	Update the template
2023-12-B2	2023-12	Increase ESD
2024-04-B3	2024-04	Modify the parameters
2025-10-B4	2025-10	Add DHVQFN16 package form

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1、General Description

The AiP74HC/HCT165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input ($\overline{PL}$) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When $\overline{PL}$ is HIGH data enters the register serially at DS. When the clock enable input ($\overline{CE}$) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on $\overline{CE}$ will disable the CP input. Inputs are overvoltage tolerant to 15V. This enables the device to be used in HIGH-to-LOW level shifting applications.

Features:

- Input levels:
  For AiP74HC165: CMOS level
  For AiP74HCT165: TTL level
- Asynchronous 8-bit parallel load
- Synchronous serial input
- ESD-HBM:3000V
- ESD-CDM:1000V
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16/DHVQFN16

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Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC165DA16.TB	DIP16	AiP74HC165	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT165DA16.TB	DIP16	74HCT165	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC165SA16.TB	SOP16	AiP74HC165	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HCT165SA16.TB	SOP16	74HCT165	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC165TA16.TB	TSSOP16	74HC165	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT165TA16.TB	TSSOP16	74HCT165	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

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Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC165SA16.TR	SOP16	AiP74HC165	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HCT165SA16.TR	SOP16	74HCT165	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC165TA16.TR	TSSOP16	74HC165	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT165TA16.TR	TSSOP16	74HCT165	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HC165QE16.TR	DHVQFN16	74HC165	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.5mm×2.5mm Pin spacing: 0.50mm
AiP74HCT165QE16.TR	DHVQFN16	74HCT165	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.5mm×2.5mm Pin spacing: 0.50mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

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2、Block Diagram And Pin Description

2.1、Block Diagram

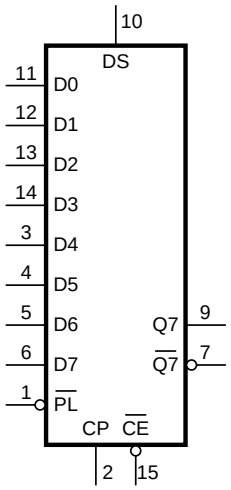


Figure 1. Logic symbol

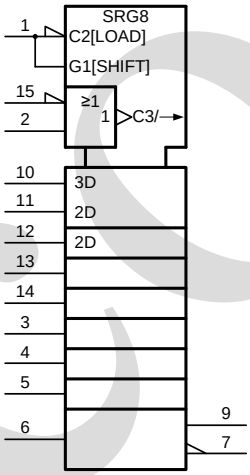


Figure 2. IEC logic symbol

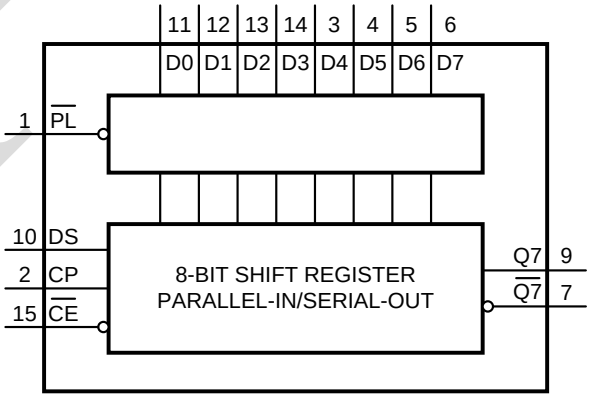


Figure 3. Functional diagram

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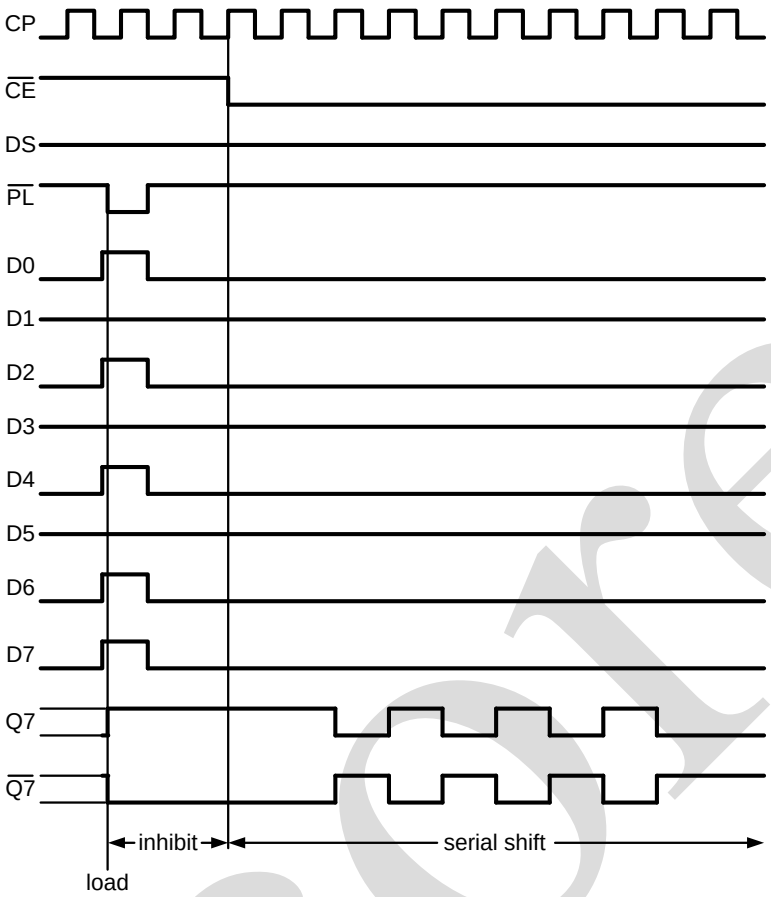
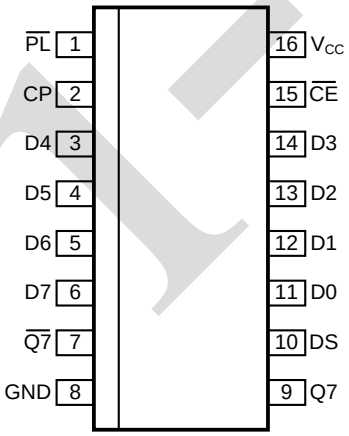
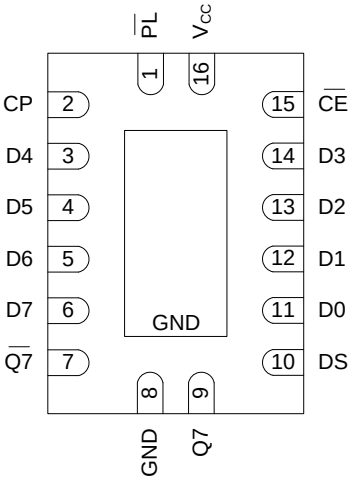


Figure 4. Timing diagram

2.2、Pin Configurations



DIP16/SOP16/TSSOP16



DHVQFN16

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2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3	D4	parallel data input (also referred to as Dn)
4	D5	parallel data input (also referred to as Dn)
5	D6	parallel data input (also referred to as Dn)
6	D7	parallel data input (also referred to as Dn)
7	$\overline{Q7}$	complementary output from the last stage
8	GND	ground (0V)
9	Q7	serial output from the last stage
10	DS	serial data input
11	D0	parallel data input (also referred to as Dn)
12	D1	parallel data input (also referred to as Dn)
13	D2	parallel data input (also referred to as Dn)
14	D3	parallel data input (also referred to as Dn)
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	supply voltage

2.4、Function Table

Operating mode	Input					Qn register		Output	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

Note:

H=HIGH voltage level;

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L=LOW voltage level;

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

X=don't care;

↑=LOW-to-HIGH clock transition.

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3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-50	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP/DHVQFN	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC165						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
AiP74HCT165						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

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3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I= V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I= V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA
input capacitance	C_I	-		-	3.5	-	pF
AiP74HCT165							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	35	126	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	65	234	uA
input capacitance	C_I	-		-	3.5	-	pF

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3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
AiP74HCT165							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	-	157.5	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	-	292.5	uA

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3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
AiP74HCT165							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	-	171.5	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	-	318.5	uA

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3.3.4、AC Characteristics 1

(T_{amb}=25℃, GND=0V, C_L=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=2.0V	-	52	165	ns
			V_{CC}=4.5V	-	19	33	ns
			V_{CC}=5.0V;C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	28	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=2.0V	-	50	165	ns
			V_{CC}=4.5V	-	18	33	ns
			V_{CC}=5.0V;C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	28	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=2.0V	-	36	120	ns
			V_{CC}=4.5V	-	13	35	ns
			V_{CC}=5.0V;C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	10	32	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=2.0V	100	22	-	ns
			V_{CC}=4.5V	20	8	-	ns
			V_{CC}=6.0V	17	6	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=2.0V	80	11	-	ns
			V_{CC}=4.5V	16	4	-	ns
			V_{CC}=6.0V	14	3	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=2.0V	5	2	-	ns
			V_{CC}=4.5V	5	2	-	ns
			V_{CC}=6.0V	5	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	5	-17	-	ns
			V_{CC}=4.5V	5	-6	-	ns
			V_{CC}=6.0V	5	-5	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	6	17	-	MHz
			V_{CC}=4.5V	30	-	-	MHz

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			V_{CC}=5.0V;C_L=15pF	32	-	-	MHz
			V_{CC}=6.0V	35	-	-	MHz
AiP74HCT165							
propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=4.5V	-	17	34	ns
			V_{CC}=5.0V;C_L=15pF	-	14	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	20	40	ns
			V_{CC}=5.0V;C_L=15pF	-	17	-	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=4.5V	-	14	35	ns
			V_{CC}=5.0V;C_L=15pF	-	11	-	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=4.5V	-	7	15	ns
pulse width	t_W	CP input; see Figure 6	V_{CC}=4.5V	16	6	-	ns
		$\overline{PL}$ input; see Figure 7	V_{CC}=4.5V	20	9	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=4.5V	20	8	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=4.5V	20	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	20	7	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=4.5V	20	10	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=4.5V	7	-1	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	0	-7	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	26	-	-	MHz
			V_{CC}=5.0V;C_L=15pF	28	-	-	MHz

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3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V, C_L=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=2.0V	-	-	150	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	35	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
AiP74HCT165							

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propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=4.5V	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	-	50	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=4.5V	-	-	38	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=4.5V	-	-	19	ns
pulse width	t_W	CP input; see Figure 6	V_{CC}=4.5V	20	-	-	ns
		$\overline{PL}$ input; see Figure 7	V_{CC}=4.5V	25	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=4.5V	25	-	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=4.5V	25	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	25	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=4.5V	25	-	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=4.5V	9	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	0	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	21	-	-	MHz

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3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +125℃, GND=0V, C_L=50pf, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC165							
propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=2.0V	-	-	250	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=2.0V	-	-	250	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=2.0V	-	-	180	ns
			V_{CC}=4.5V	-	-	42	ns
			V_{CC}=6.0V	-	-	38	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	CP input HIGH or LOW; see Figure 6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{PL}$ input LOW; see Figure 7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
AiP74HCT165							

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propagation delay	t_{PLH}, t_{PHL}	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; see Figure 6	V_{CC}=4.5V	-	-	51	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; see Figure 7	V_{CC}=4.5V	-	-	60	ns
		D7 to Q7, $\overline{Q7}$; see Figure 8	V_{CC}=4.5V	-	-	42	ns
transition time	t_{THL}, t_{TLH}	Q7, $\overline{Q7}$ output; see Figure 6	V_{CC}=4.5V	-	-	22	ns
pulse width	t_W	CP input; see Figure 6	V_{CC}=4.5V	24	-	-	ns
		$\overline{PL}$ input; see Figure 7	V_{CC}=4.5V	30	-	-	ns
recovery time	t_{rec}	$\overline{PL}$ to CP, $\overline{CE}$; see Figure 7	V_{CC}=4.5V	30	-	-	ns
set-up time	t_{su}	DS to CP, $\overline{CE}$; see Figure 9	V_{CC}=4.5V	30	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	30	-	-	ns
		Dn to $\overline{PL}$; see Figure 10	V_{CC}=4.5V	30	-	-	ns
hold time	t_h	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; see Figure 9	V_{CC}=4.5V	11	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; see Figure 9	V_{CC}=4.5V	0	-	-	ns
maximum frequency	f_{max}	CP input; see Figure 6	V_{CC}=4.5V	17	-	-	MHz

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4、Testing Circuit

4.1、AC Testing Circuit

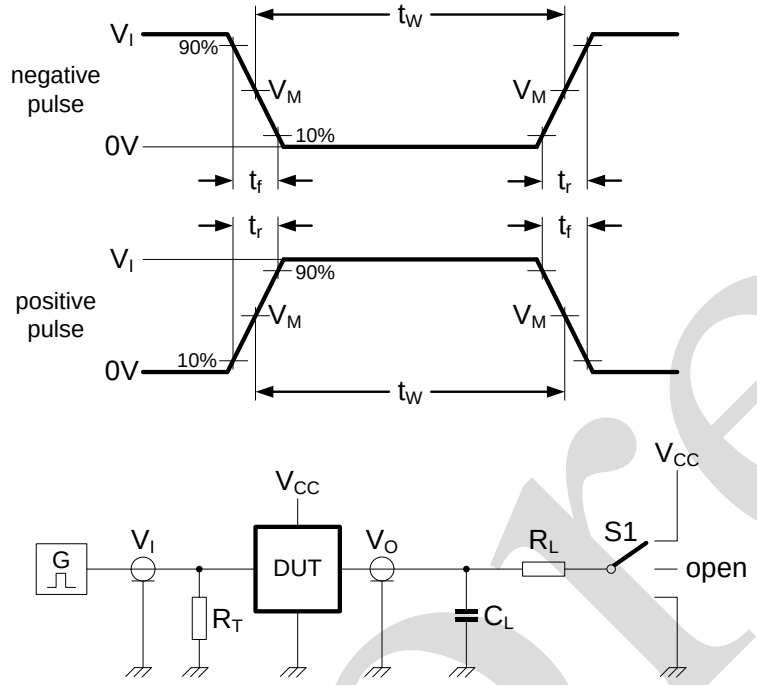


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

RL=Load resistance.

S1=Test selection switch.

4.2、AC Testing Waveforms

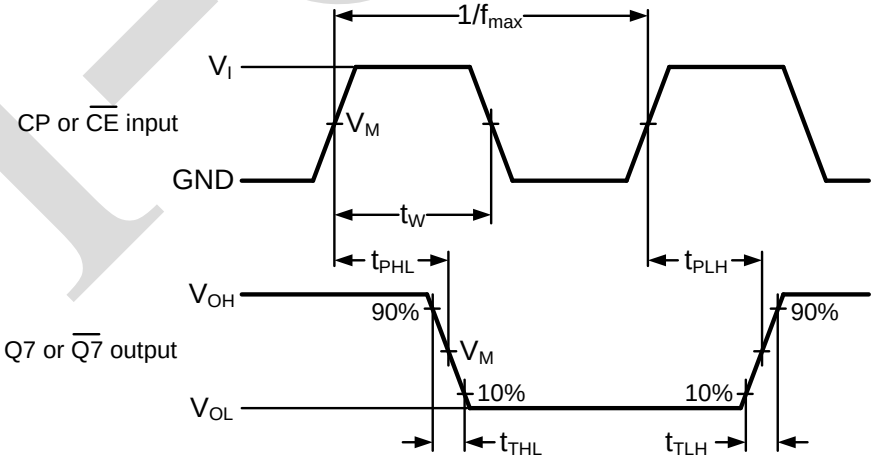


Figure 6. The clock (CP) or clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times

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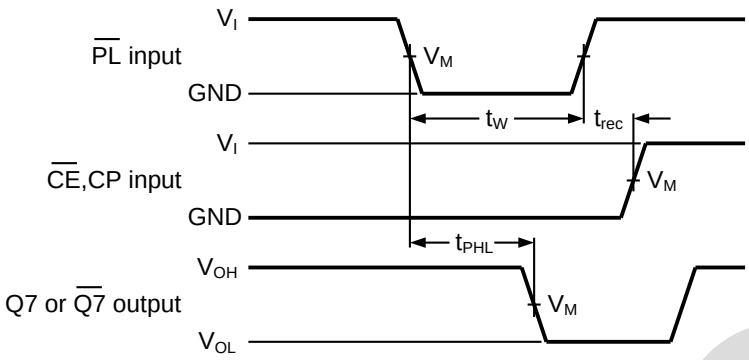


Figure 7. The parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time

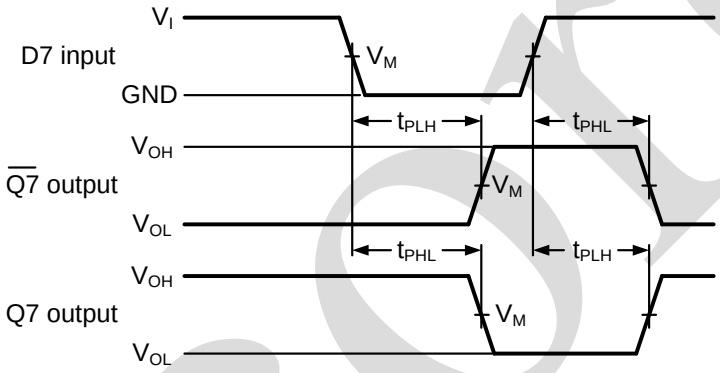
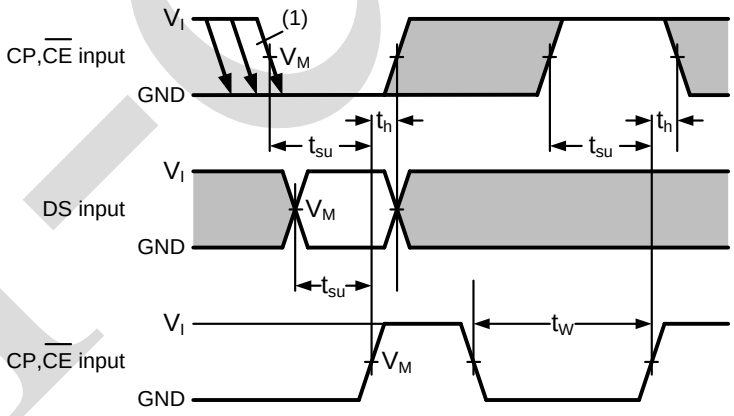


Figure 8. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW



(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

Figure 9. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$)

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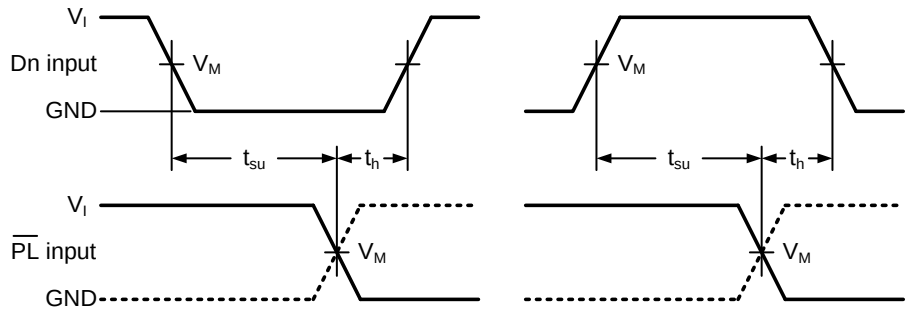


Figure 10. The set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

4.3、Measurement Points

Type	Input		Output
	V_I	V_M	V_M
AiP74HC165	V_{CC}	$0.5\times V_{CC}$	$0.5\times V_{CC}$
AiP74HCT165	3V	1.3V	1.3V

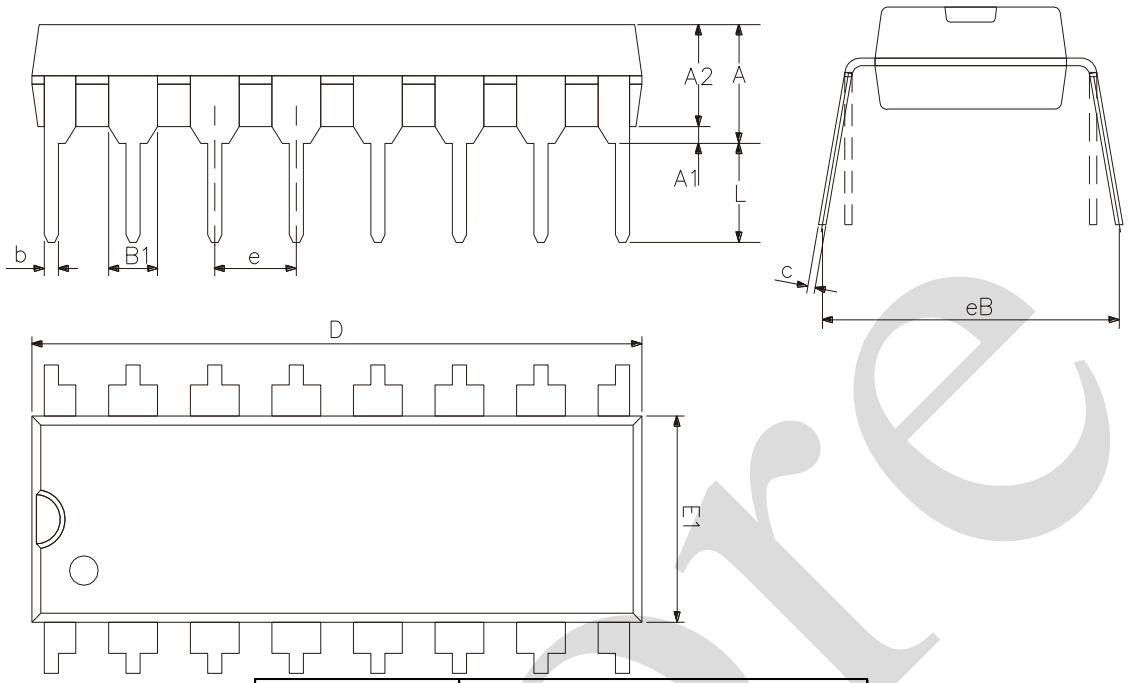
4.4、Test Data

Type	Input		Load		S1 position
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}
AiP74HC165	V_{CC}	6.0ns	15pF, 50pF	1kΩ	open
AiP74HCT165	3.0V	6.0ns	15pF, 50pF	1kΩ	open

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5、Package Information

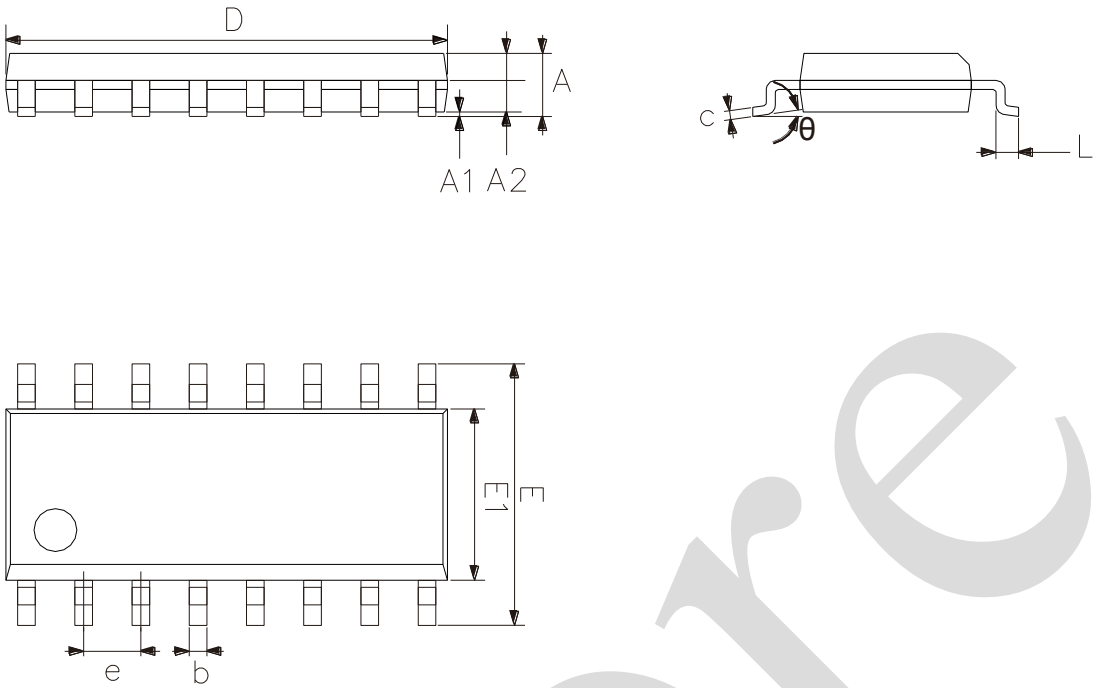
5.1、DIP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A2	3.20	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	—
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

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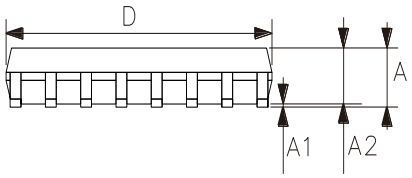
5.2、SOP16

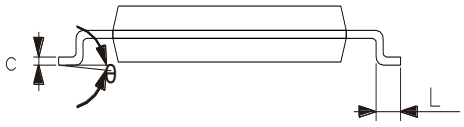


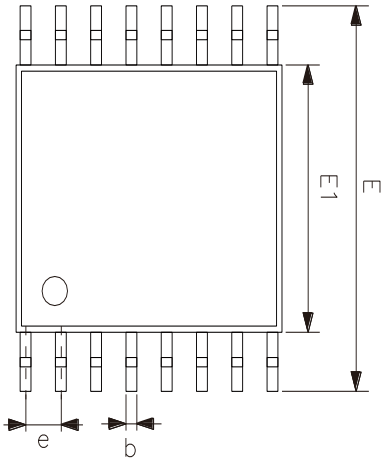
2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

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5.3、TSSOP16



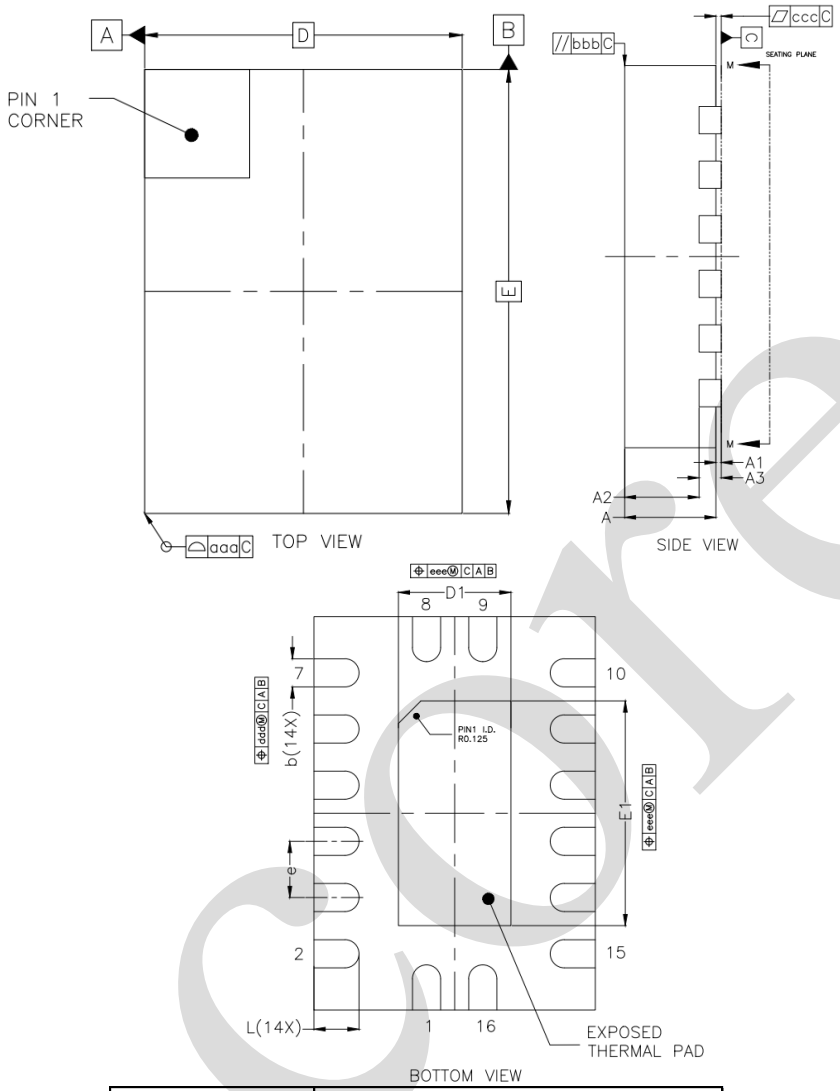




2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

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5.4、DHVQFN16



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	2.40	2.60
E	3.40	3.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	0.85	1.15
E1	1.85	2.15

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6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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